WHAT IS CLAIMED IS:

SUB B1

1. A method of manufacturing a semiconductor device, the method comprising:

forming a first dielectric layer overlying a substrate;

forming a first barrier layer, comprising a first dielectric barrier material, on the first dielectric layer;

etching to form a first opening defined by side surfaces of the first dielectric layer and a bottom;

forming a second barrier layer, comprising a second dielectric barrier material different from the first dielectric barrier material, on an upper surface of the first barrier layer overlying the first dielectric layer, on the side surfaces of the first dielectric layer defining the first opening and on the bottom of the opening;

etching, with selectivity to the first barrier layer, to remove the second barrier layer from, and stopping on, the upper surface of the first barrier layer, and to remove the second barrier layer from the bottom of the first opening, leaving a portion of the second barrier layer as a liner on the side surfaces of the first dielectric layer defining the first opening; and

filling the opening with metal to form a lower metal feature.

2. The method according to claim 1, wherein the first and second dielectric barrier materials are selected from the group consisting of silicon nitride, silicon oxynitride and silicon carbide.

3. The method according to claim 2, comprising depositing each of the first and second barrier layers by chemical vapor deposition.

4. The method according to claim 3, comprising depositing each of the first and second barrier layers at a thickness of about 50Å to about 500Å.

5. The method according to claim 1, comprising filling the opening with copper (Cu) or a Cu alloy.

SUB B2

6. The method according to claim 1, further comprising:

forming a third barrier layer, comprising a third dielectric barrier material different from the first dielectric barrier material, on the first barrier layer and on an upper surface of the lower metal feature;

forming a second dielectric layer on the third barrier layer;

forming a fourth barrier layer, comprising a fourth dielectric barrier material, on the second dielectric layer;

forming a third dielectric layer on the fourth barrier layer;

forming a fifth barrier layer, comprising a fifth dielectric barrier material, on the third dielectric layer;

etching to form a dual damascene opening comprising an upper trench portion defined by side surfaces of the third dielectric layer in communication with a lower via hole defined by side surfaces of the second dielectric layer and a bottom on at least a portion of the upper surface of the lower metal feature;

forming a sixth barrier layer, comprising a sixth dielectric barrier material different from the first, fourth and fifth dielectric materials, on the fifth barrier layer overlying the third dielectric layer, on the side surfaces of the third dielectric layer defining the trench, on the side surfaces of the second dielectric layer defining the via hole, on a portion of the fourth barrier layer between the trench and via hole, and at the bottom of the via hole;

etching to remove the sixth barrier layer from, and stopping on, the fifth barrier layer, from and stopping on the fourth barrier layer, and at the bottom of the via hole, leaving a portion of the sixth barrier layer as a liner on the side surfaces of the third dielectric layer defining the trench and on the side surfaces of the second dielectric layer defining the via hole; and

filling the dual damascene opening with metal to form a metal line connected to an underlying metal via.

7. The method according to claim 6, comprising filling the dual damascene opening with copper (Cu) or a Cu alloy to form a Cu or Cu alloy line connected to a Cu or Cu via which is electrically connected to the lower metal feature.

8. The method according to claim 7, wherein the lower metal feature comprises a Cu or Cu alloy line.

9. The method according to claim 7, wherein the dual damascene opening is misaligned with respect to the lower metal feature such that the bottom of the via hole is on a portion of the upper surface of the lower metal feature and on a portion of an upper surface of the first barrier layer.

10. The method according to claim 6, further comprising depositing a seventh barrier layer, comprising a seventh dielectric barrier material, on an upper surface of the sixth barrier layer and on an upper surface of the metal line.

11. The method according to claim 6, wherein the first, second, third, fourth, fifth and sixth dielectric barrier materials are selected from the group consisting of silicon nitride, silicon carbide and silicon oxynitride.

12. The method according to claim 6, comprising depositing each of the first, second, third, fourth, fifth and sixth barrier layers at a thickness of about 50Å to about 500Å.

13. A semiconductor device comprising:

a lower metal feature, comprising copper (Cu) or a Cu alloy, formed in an opening defined by side surfaces of a first dielectric layer having a first barrier layer, comprising a first dielectric barrier material, thereon;

a first barrier liner, comprising a second dielectric barrier material different from the first dielectric barrier material, on the side surfaces of the first dielectric layer between the lower metal feature and the first dielectric layer, the first barrier liner having an upper surface extending to a distance below an upper surface of the first dielectric layer.

14. The semiconductor device according to claim 13, wherein the distance between the upper surface of the first barrier liner and the upper surface of the first barrier layer is about 25Å to about 200Å.

15. The semiconductor device according to claim 13, further comprising:

a second barrier layer, comprising a third dielectric barrier material different from the first dielectric barrier material, on the first barrier layer overlying the first dielectric layer; and

a dual damascene structure formed on and electrically connected to the lower metal feature, the dual damascene structure comprising:

a second dielectric layer on the second barrier layer;

a third barrier layer, comprising a fourth dielectric barrier material, on the second dielectric layer;

a third dielectric layer on the third barrier layer;

a fourth barrier layer, comprising a fifth dielectric barrier layer material, on the third dielectric layer;

a dual damascene opening comprising a trench, defined by side surfaces of the third dielectric layer, connected to a via hole, defined by side surfaces of the second dielectric layer and a bottom on at least a portion of the upper surface of the lower metal feature;

a second barrier liner, comprising a sixth dielectric barrier material different from the first, fourth and fifth dielectric barrier materials, on the side surfaces of the second dielectric layer defining the via hole and on the side surfaces of the third dielectric layer defining the trench ; and

Cu or a Cu alloy filling the dual damascene opening and forming a Cu or Cu alloy line in the third dielectric layer connected to a via in the second dielectric layer which, in turn, is electrically connected to the lower metal feature.

16. The semiconductor device according to claim 15, wherein:

an upper surface of the second barrier liner on the side surfaces of the second dielectric layer extends to a distance below the upper surface of the third barrier layer; and

an upper surface of the second barrier liner on the side surfaces of the third dielectric layer extends to a distance below the upper surface of the fourth barrier layer.

17. The semiconductor device according to claim 16, wherein:

the distance between the upper surface of the second barrier liner on the side surfaces of the second dielectric layer and the upper surface of the third barrier layer is about 25Å to about 200Å; and

the distance between the upper surface of the second barrier liner on the side surfaces of the third dielectric layer and the upper surface of the fourth barrier layer is about 25Å to about 200Å.

18. The semiconductor device according to claim 15, wherein the dual damascene opening is misaligned with respect to the lower metal feature such that the bottom of the via hole is on a portion of the upper surface of the lower metal feature and on a portion of an upper surface of the first barrier layer.

19. The semiconductor device according to claim 15, wherein the first and second barrier liners and the first, second, third and fourth barrier layers each have a thickness of about 50Å to about 500Å.

20. The semiconductor device according to claim 15, wherein the first, second, third, fourth, fifth and sixth dielectric barrier materials are selected from the group consisting of silicon nitride, silicon carbide and silicon oxynitride.

ADD B3>